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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,403	01/26/2004	Ho-young Song	5649-1180	2218

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/765,403	SONG, HO-YOUNG	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,29-40 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-27 and 29-35* is/are allowed.

6)☒ Claim(s) *1-6,9,12,15-19,36,37,39 and 43* is/are rejected.

7)☒ Claim(s) *7,8,10,11,13,14,38 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed 10-19-2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 15-19, 36 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. (US PAT No. 5,729,152).

Regarding claims 1 and 15, Fig.20a of Leung et al. teaches a termination circuit for a transmission line and a method of terminating a transmission line (2002;col. 6, lines 49-50, col. 28, lines 38-44), the termination circuit comprising: an input node (THE NODE coupled to bus 2030) receiving an input signal (Data_In) over the transmission line (2030); a pull-down circuit (2007) coupled between the input node and a first reference voltage (Ground) wherein the pull-down circuit is configured to provide an electrical path (path from the node to the Ground) between the first reference voltage and the input node responsive to the input signal (when input signal at the node is logic high, is turned on via I3 and I4)having a first voltage level; and a pull-up circuit (2006) coupled between the input node (THE NODE) and a second reference voltage (VDD) wherein the pull-up circuit is configured to provide an electrical path (path from THE NODE to VDD) between the second reference voltage and the input node responsive to the input signal having a second voltage level (when input signal at THE NODE is logic

low, 2006 is turned), wherein the first reference voltage is less than the second reference voltage (Ground is less than VDD) and wherein the first voltage level is greater than the second voltage level (logic high is greater than logic low) wherein the pull-down circuit maintains the electrical path between the first reference voltage and the input node while the input signal is maintained steady state at the first voltage level (as long as the input signal at THE NODE is logic high, 2007 remains to be turned on); wherein the pull-up circuit maintains the electrical path between the second reference voltage and the input node while the input signal is maintained steady state at the second voltage level (as long as the input signal at THE NODE is logic low, 2006 remains to be turned on).

Regarding claims 2 and 16, Fig.20a of Leung et al. teaches a termination circuit according to claim 1 and the method according to claim 15 wherein the first voltage level comprises a logic high voltage level (logic high at THE NODE turns on 2007) and wherein the second voltage level comprises a logic low voltage level (a logic low at THE NODE turns on 2006).

Regarding claims 3 and 17, Fig.20a of Leung et al. teaches a termination circuit according to claim 1 and the method according to claim 15 wherein the first reference voltage comprises a ground voltage (2007 is coupled to ground) and the second reference voltage comprises a supply voltage (VDD is the supply voltage).

Regarding claims 4 and 18, Fig.20a of Leung et al. teaches a termination circuit according to claims 1 and the method according to claim 15 wherein: the pull-down circuit is further configured to block the electrical path between the first reference voltage and the input node responsive to the input signal having the second voltage level (when the input voltage at THE NODE is logic low, 2007 is turned off); and the pull-up circuit is further configured to block the electrical current path between the second reference voltage and the input node responsive to the input signal having the first voltage level (when the input voltage at THE NODE is logic high, 2006 is turned off).

Regarding claims 5 and 19, Fig. 20a of Leung et al. teaches a termination circuit according to claim 4 and the method according to claim 18 wherein the pull-down and pull-up circuits are further configured to provide electrical paths between the input node and both of the first and second reference voltages at a same time during a transition of the input signal between the first and second voltage levels (when the current through 2006 and 2007 is about the same during the transition, both 2006 and 2007 are turned on and provides electrical paths at the same time, col. 28, lines 4-13).

Regarding claim 36, Fig. 20a of Leung et al. teaches a termination circuit which reduces ringing and dynamic current (col. 28, lines 38-51), which occur when an input signal is transmitted through a transmission line to an input node (NODE coupled to 2030), the termination circuit comprising: a pull-down unit (2007) which prevents a

voltage level at the input node from reaching a voltage level of a second voltage (VDD) when a voltage level of the input signal at the input node is at a first level (logic high level, e.g. when input signal at the NODE is logic high, 2007 is turned on and pulls the node to ground preventing the NODE rising to VDD); and a pull-up unit (2006) which prevents a voltage level at the input node from reaching a voltage level of a first voltage (ground) when a voltage level of the input signal at the input node is at a second level (logic low, e.g. when input signal at the NODE is logic low, 2006 is turned on and pulls up the NODE to VDD preventing the NODE falling to ground), where a voltage level of the first voltage (ground) is the same as a voltage level of a ground voltage and a voltage level of the second voltage (VDD) is the same as a voltage level of a supply voltage where the first level (logic high) is high and the second level (logic low) is low.

Regarding claim 43, Fig. 20a of Leung et al. teaches the termination circuit of claim 36, wherein the termination circuit is mounted in a semiconductor chip (Fig. 19 shows multiple memory devices where Fig. 20a is being implemented).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. in view of Volk (US PAT No. 6,356,105).

Regarding claims 6, 9 and 12, Leung et al. teaches a termination circuit according to claim 1 where the transistors 2006 and 2007 are sized to suppress reflections and ringing (col. 28, lines 42-51), but does not teach a pull-down resistor in series between the input node and the first reference voltage nor a pull-up resistor in series between the input node and the second reference voltage. However, Fig. 5 of Volk teaches a pull-down resistor in series between the input node and the first reference voltage and a pull-up resistor in series between the input node and the second reference voltage for the purpose of providing linear impedance compensation of the buffer. It would have been obvious at the time of invention to modify the sized pull-down and pull-up transistors with the pull-down and pull-up transistors in series with a respective resistors since it would provide improved compensation of termination impedance.

Claims 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. in view of Volk (US PAT No. 6,356,105) and Kumar (US PAT No. 5,426,383).

Regarding claims 37 and 39, Leung et al. teaches a termination circuit according to claim 36 where the pull up NMOS 2006 and the pull down PMOS 2007 with a common inverter 2020 are sized to suppress reflections and ringing (col. 28, lines 42-51), but does not teach the pull down unit comprising an NMOS and the pull up unit comprising a PMOS, and a pull-down resistor in series between the input node and the

first reference voltage nor a pull-up resistor in series between the input node and the second reference voltage and . However, Figs. 10A and 10C of Kumar teaches the PMOS transistor (25 in Fig. 10A) replaceable with an inverter (53 in Fig. 10C) in series with an NMOS (56 in Fig. 10C), based on the speed requirement (col. 7, lines 56-66). It would have been obvious at the time of invention to replace the NMOS (2006) having an inverter (2020) with a PMOS of Kumar and the PMOS (2007) with an NMOS having an inverter of Kumar in order to accommodate faster or slow switching speed, and Fig. 5 of Volk teaches a pull-down resistor in series between the input node and the first reference voltage and a pull-up resistor in series between the input node and the second reference voltage for the purpose of providing linear impedance compensation of the buffer. It would have been obvious at the time of invention to modify the sized pull-down and pull-up transistors with the pull-down and pull-up transistors in series with a respective resistors since it would provide improved compensation of termination impedance.

Allowable Subject Matter

Claims 20-27 and 29-35 are allowable over the prior art of record.

Claims 7-8,10-11,13-14,38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach, among other things, the specific of the termination resistance of the first and second switching units being maintained level to

a resistance of the transmission when the voltage level of the input signal is changed (claims 20 and 30), and a first input resistor connected between the input node and a control electrode of the pull-down transistor (claims 7, 13 and 38), a pull-up input resistor connected between the input node and a control electrode of the pull-up transistor (claims 9, 13 and 40).

Response to Arguments

Applicant's arguments with respect to claims 20-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Thursday 5:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 1-6-2005